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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,190	06/30/2003	Bruce B. Doris	FIS920030152	1189

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,190	DORIS ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *18-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 13-17* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group I (Claims 1-17) drawn to a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 18-20 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5-9, 13-17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,512,273 to Krivokapic et al. in view of Huang et al. (US 2004/0104405).

Regarding to claims 1, 7-8, Krivokapic discloses a semiconductor device structure (see the entire patent, including the Fig. 2 disclosure), comprising: at least first and second field effect transistors disposed on a substrate 2; first field effect transistor including a first spacer 33 having a first width; second field effect transistor including a second spacer 20/33 having a second width.

Krivokapic does not disclose the second spacer includes a first compressive stress material, and the structure further comprises a tensile stress material disposed on at least first and second field effect transistors.

However, Huang et al. teach the second spacer includes a first compressive stress material 40', and the structure further comprises a tensile stress material 50' disposed on at least first and second field effect transistors (page 2, paragraph [0042]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second spacer includes a first compressive stress material, and the structure further comprises a tensile stress material disposed on at least first and second field effect transistors, as taught by Huang et al. in order to provide a MOS/CMOS device having different stresses on at least two different areas (page 1, paragraph [0012]).

Regarding to claim 2, Krivokapic discloses the structure wherein first field effect transistor is an nFET and second field effect transistor is a pFET (fig. 1).

Regarding to claim 3, Krivokapic discloses the structure wherein first width is less than second width (fig. 1).

Claim 4 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,512,273 to Krivokapic et al. in view of Huang et al. (US 2004/0104405) and further in view of Ogoh (5,254,866).

Regarding to claim 4, Krivokapic et al. in view of Huang et al. disclose the claimed invention except for the structure is an inverter. Ogoh teaches that CMOS transistors are conventionally used to form a CMOS inverter (col. 12, lines 6-9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an inverter, as taught by Ogoh in order to provide a structure of a semiconductor device including a MOS-LDD field effect transistor circuit in which widths can be varied with side wall spacers as masks for adjusting distribution of impurity concentration at need in a relatively short CVD processing time (col. 4, lines 3-9).

Claims 5-6 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,512,273 to Krivokapic et al. in view of Huang et al. (US 2004/0104405) and in view of Ogoh (5,254,866), and further in view of Frenette et al. (6,028,339).

Regarding to claim 5, Frenette discloses the structure includes a width transition region located approximately in a middle region between transistors (fig. 4).

Regarding to claim 6, Frenette discloses the structure wherein the first spacer 34 includes an I-shaped part and the second spacer 30/32/34 includes an L-shaped part.

Claims 9, 16-17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,512,273 to Krivokapic et al. in view of Huang et al. (US 2004/0104405), Ogoh (5,254,866), Frenette et al. (6,028,339), Chang et al. (6,222,238), and further in view of Yang et al. (6,548,877).

Yang teaches that gate spacers are conventionally 10 nm to 50 nm wide (see col. 4, lines 7-15). It would have been obvious to one skilled in this art to make Chang's spacers 10 nm to 50 nm wide, because such spacers are conventionally that wide, as taught by Yang.

Regarding to claim 13, Huang discloses the structure wherein the first compressive stress material is a dielectric (page 2, paragraph [0043]).

Regarding to claim 14, Huang discloses the structure wherein the first compressive stress material is silicon nitride (page 2, paragraph [0043]).

Regarding to claim 15, Huang discloses the structure wherein the tensile stress material is SiN (page 2, paragraph [0043]).

Allowable Subject Matter

Claims 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran

Date : 7/22/04

David Nelms
Supervisory Patent Examiner
Technology Center 2800